REMARKS

Claims 11, 20, and 29 have been canceled. Claims 1-10, 12-19 and 21-28 are pending and each of these claims has been amended. No new matter has been added to the amended claims. Support for the amendments can be found in the specification.

Claims Rejections Under 35 U.S.C. § 112

Claims 20 and 29 were rejected under 35 U.S.C. § 112. Claims 20 and 29 have been canceled.

Claim Rejections Under 35 U.S.C. §§ 102 and 103

Claims 1-29 were rejected as being anticipated by or obvious in light of Japanese patent 61-254078 to Muramoto and U.S. Patent 6,157,242 to Fukui.

Claims 1-10, 12-19, and 21-28 have been amended to address these rejections.

Claims 1 and 12

Independent claim 1, for example, has been amended to recite

> a first native transistor;
> first depletion transistors coupled together and to the first native transistor in series, each of the first depletion transistors having a threshold voltage that is lower that a threshold voltage of the first native transistor at a common source voltage; and
> first capacitors, wherein a drain of each of the first depletion transistors is coupled to one of the first capacitors, a first subset of the first capacitors are coupled to receive a first clock signal, and a second subset of the first capacitors are coupled to receive a second clock signal.

Neither Fukui nor Muramoto disclose or suggest charge pump with a native transistor and depletion transistors. A native transistor does not have a threshold voltage implant in the channel of the device. As a result, a native transistor has a low threshold voltage (e.g., 0.3 volts or less). See FIG. 2 of the present application and page 3, paragraph 15.

Muramoto discloses a circuit that has N-type enhancement MOS transistors. See abstract of Muramoto. An enhancement FET has a positive threshold voltage implant in the channel region of the device. The positive threshold voltage implant raises the threshold voltage of the device (e.g., to 0.7 volts).

A charge pump circuit that has an enhancement FET coupled between the input and the output cannot pump a very low input voltage (e.g., 1.4 volts) to a very high output voltage (e.g., 15 volts). For example, when the drain and gate bias of the enhancement FET is increased from 1.4 volts to about 2.7 volts, the threshold voltage of the enhancement FET increases from 0.7 volts to about 1.2 volts. At a supply voltage of 1.4 volts at the source of the FET, the transistor would be nearly OFF, because the gate-source voltage would be close to the threshold voltage. If the enhancement FET is OFF, it cannot conduct current to the output.

For these reasons claim 1 and its dependent claims are novel and nonobvious over the cited references. Claim 12 and its dependent claims are allowable for similar reasons.

Claims 2, 13, and 21

Claim 21, for example, has been amended to recite:

> a first native transistor;
> first depletion transistors each having a threshold voltage that is lower that a threshold voltage of the first native transistor at a common source voltage;
> second depletion transistors each having a threshold voltage that is lower than the threshold voltage of each of the first depletion transistors at a common source voltage.

Neither Fukui nor Muramoto disclose or suggest a charge pump with first and second sets of depletion transistors, wherein the second set of depletion transistors have lower threshold voltages than the first set of depletion transistors.

Having a second set of depletion transistors with a lower threshold voltage provides a greater incremental voltage across the highest charge pump stages, allowing the charge pump to boost the output voltage to a greater value. See the present application at page 10, line 33 - page 11, line 16.

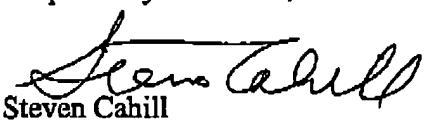
For at least these reasons, it is respectfully submitted that amended claim 21 is novel and nonobvious over the cited references. Amended claims 2 and 13 are also allowable for similar reasons.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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